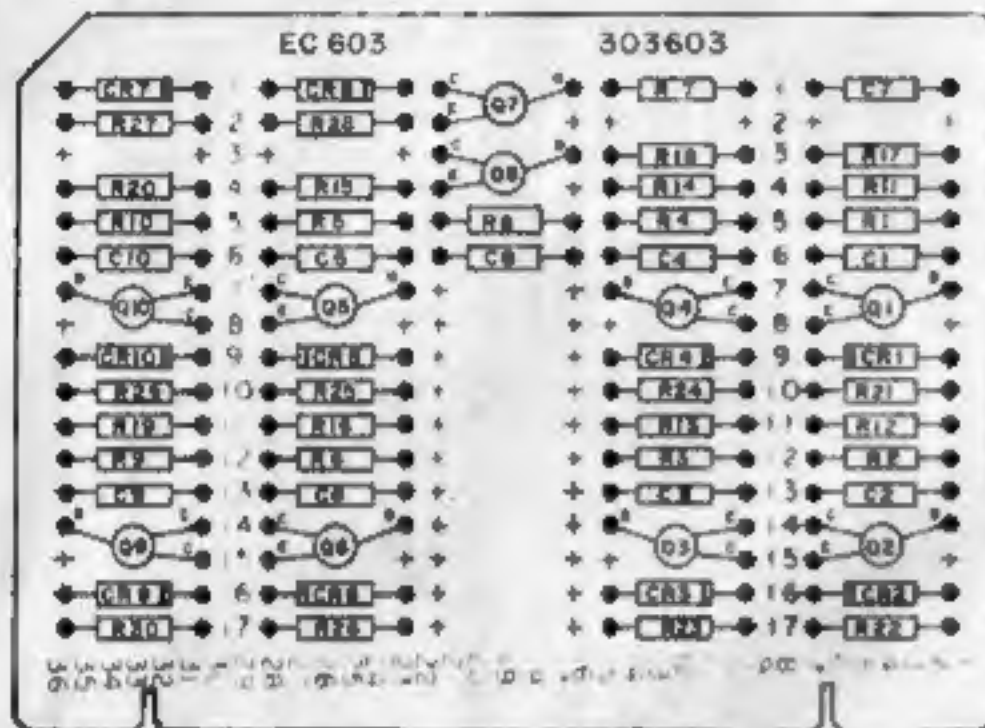
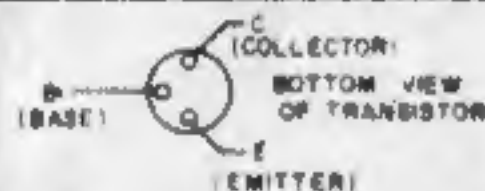


EC603
303603



NOTE
REFER TO 6100 WD FOR BASIC MARKING INFORMATION.



THIS CARD CONSISTS OF TEN IDENTICAL CIRCUITS. WHEN TERMINALS ② ARE TIED TO 0 VOLTS, THE CIRCUIT ACTS AS AN INVERTER. WHEN TERMINALS ② ARE USED AS INPUTS, THE CIRCUIT ACTS AS AN INHIBIT GATE.

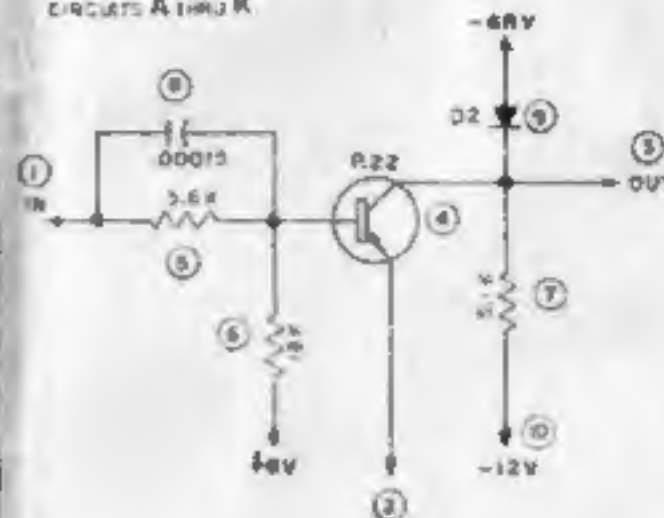
INVERTER OPERATION WHEN 0 VOLTS IS APPLIED AT INPUT TERMINAL ① TRANSISTOR ④ IS IN CUT-OFF CAUSING OUTPUT TERMINAL ③ TO BE CLAMPED AT -6 VOLTS. WHEN -6 VOLTS IS APPLIED AT INPUT TERMINAL ①, TRANSISTOR ④ SATURATES CAUSING OUTPUT TERMINAL ③ TO BE APPROXIMATELY -0.3 VOLTS. SPEED-UP CAPACITOR ⑧ IMPROVES OUTPUT SIGNAL RISE TIME.

INHIBIT GATE OPERATION INPUT TERMINALS ① AND ② VARY BETWEEN 0 VOLTS AND -6 VOLTS. WHEN INPUT TERMINAL ② IS AT -6 VOLTS, TRANSISTOR ④ IS IN CUT-OFF CAUSING TERMINAL ③ TO BE CLAMPED AT -6 VOLTS. INDEPENDENT OF VOLTAGE AT INPUT TERMINAL ①. WHEN INPUT TERMINAL ② IS AT 0 VOLTS, THE CIRCUIT DESCRIPTION IS THE SAME AS THE INVERTER DESCRIBED ABOVE.

THE COLLECTOR VOLTAGE (-12V) IS BROUGHT OUT AT THREE SEPARATE TERMINALS AS SHOWN TO THE RIGHT. THIS WILL ENABLE DELETING COLLECTOR VOLTAGES ON CERTAIN INVERTERS OR INHIBIT GATES, SO THAT MULTIPLE CIRCUITS

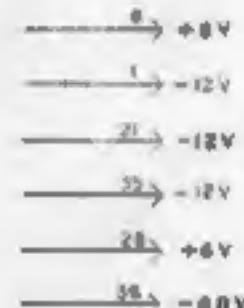
INHIBIT GATE OR INVERTER (10)

CIRCUITS A THRU K



NOTE

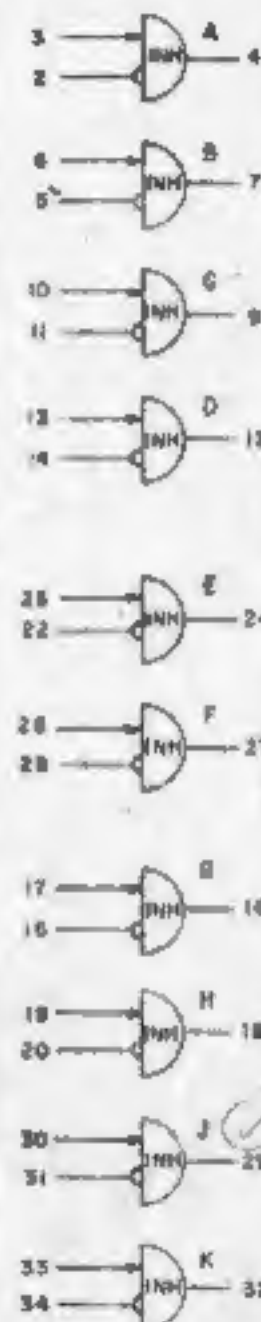
CIRCLED NUMBERS DESIGNATE COMPONENTS OR INPUT AND OUTPUT TERMINALS ON MULTIPLE CIRCUITS.



TABLE

	①	②	③	④	⑤	⑥	⑦	⑧	⑨	⑩
A	2	3	4	Q1	R1	R11	R21	C1	CR1	1
B	5	6	7	Q2	R2	R12	R22	C2	CR2	1
C	11	10	9	Q3	R3	R13	R23	C3	CR3	1
D	14	13	12	Q4	R4	R14	R24	C4	CR4	1
E	22	23	24	Q5	R5	R15	R25	C5	CR5	21
F	25	26	27	Q6	R6	R16	R26	C6	CR6	21
G	18	17	16	Q7	R7	R17	R27	C7	CR7	35
H	20	19	18	Q8	R8	R18	R28	C8	CR8	35
J	31	30	29	Q9	R9	R19	R29	C9	CR9	35
K	34	33	32	Q10	R10	R20	R30	C10	CR10	35

SYMBOLS



R&D USE ONLY

